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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/774,994	02/09/2004	Christian D. Kasper	98-C-170C2 (STMI01-00082)	9590

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EXAMINER	
KENDALL, CHUCK O	

ART UNIT	PAPER NUMBER
2192	

MAIL DATE	DELIVERY MODE
07/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/774,994	KASPER, CHRISTIAN D.	
	Examiner	Art Unit	
	Chuck O. Kendall	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is in response to Application filed 02/09/04.

2. Claims 1 – 20 have been examined.

Double Patenting

3. Claims 1 – 20 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1 - 23 of U.S. Patent No. 6,691,308 B1, Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Claims 1 – 20, claim essential the same limitations as disclosed in claims 1 - 23 of the parent application, although the parent application '308 appears to be more in depth and specific.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 – 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Sheil USPN6,049,672.

Regarding claim 1, Sheill anticipates a hot patch system for changing of code in a processor comprising, in combination:

a memory for storing a plurality of instructions (FIG.1, 24);

a program counter coupled to the memory for indexing of the memory to access an instruction (23:45 – 50, see incrementing counters); and

a cache system coupled to the memory and to the program counter for comparing information associated with the instruction from memory with information stored in the cache system and for altering an instruction stream when there is a comparison match (9:35 – 40).

Regarding claim 2, hot patch system in accordance with Claim 1 wherein the cache system comprises:

a cache for storing information (FIG. 6, 84);

a register coupled to the cache for storing the information associated with the instruction from memory that is to be compared
to the information stored in the cache (FIG. 6, 110); and

cache control logic coupled to the cache for controlling insertion of one of, the instruction from the memory or an instruction from the cache system into the instruction stream (FIG. 6, 105 and all associated text).

Regarding claim 3, a hot patch system in accordance with Claim 2 further

comprising a switching device coupled to the memory, cache, and the cache control logic for inserting one of the instruction from the memory unit or the instruction from the cache system into the instruction stream (13:5 – 10, see multiplexer).

Regarding claim 4, a hot patch system in accordance with Claim 3 wherein the cache comprises a plurality of cache lines wherein each cache line has at least a first field for storing flag information, a second field for storing a cache line instruction, and a third field for

storing information which is to be compared with information stored in the register (16:5 – 10, see flags and indicate state of each cache location, i.e. cache line).

Regarding claim 5, a hot patch system in accordance with Claim 4 wherein the third field stores a memory address (FIG. 1, 24a – 24c).

Regarding claim 6, a hot patch system in accordance with Claim 4, wherein the third field stores an instruction (FIG. 1, 24b).

Regarding claim 7, a hot patch system in accordance with Claim 4 wherein the cache is one of a single direct mapped cache or a single fully associative cache (FIG. 5, 84 and all associated text).

Regarding claim 8. A hot patch system in accordance with Claim 4 wherein the cache comprises:

an address cache (FIG. 5, 84); and

an instruction cache (FIG. 5, 84, also see 90 see memory table).

Regarding claim 9, a hot patch system in accordance with Claim 2 further comprising a mask register, coupled to the cache for controlling how information

associated with the instruction from the memory is to be compared with information in the cache and for modifying the information in the cache (27:65, see mask set).

Regarding claim 10, a hot patch system in accordance with Claim 6 wherein the mask register is a global mask (27:65, interprets the mask set to include global and local masks).

Regarding claim 11, a hot patch system in accordance with Claim 6 wherein the mask register is a local mask (27:65, interprets the mask set to include global and local masks).

Regarding claim 12, a hot patch circuit in accordance with Claim 7 wherein the switching device is a multiplexer having a first input coupled to the cache, a second input coupled to the memory, and a third input coupled to the cache control logic (13:5 – 10, see multiplexer).

Regarding claim 13, a hot patch circuit in accordance with Claim 5 wherein the switching device comprises:

a first multiplexer having a first input coupled to the address cache, a second input coupled to the instruction cache, and a third input coupled to the cache control logic (FIG. 4, 87 and 88 shows two multiplexers); and

a second multiplexer having a first input coupled to an output of the first multiplexer, a second input coupled to the memory unit, and a third input coupled to the cache control logic (13:5 – 10, see multiplexer, also see FIG. 4 see items 87 and 88).

Regarding claim 14, a hot patch circuit in accordance with Claim 3 further comprising a status buffer having an input coupled to the cache, an input coupled to the

switching device and an input coupled to the cache control logic for storing information, related to the operation of the circuit (FIG. 11, see 212 and all associated text).

Regarding claim 16, Sheil anticipates a method, of altering the code of a pipeline processor comprising the steps of:

storing a plurality of instructions in memory (FIG.1, 24);

storing information in a cache (FIG. 6, 84);

indexing of the memory to access an instruction (16:65 – 67, see content addressable memory);

comparing information associated with the instruction from memory with the information in the cache (9:35 – 40); and

inserting an instruction from the cache into the instruction stream when the information associated with the instruction from memory matches the information in the cache (17:1 – 5, see patch).

Regarding claim 17, the method of Claim 16 further comprising the step of inserting the instruction from memory into the instruction stream when the information associated with the instruction from memory does not match the information in the cache (32:55 – 60, see fails to match).

Regarding claim 18, the method of Claim 16 wherein the step of storing information in the cache further comprises the step of programming a plurality of cache lines in the cache to store a first field for storing flag information, a second field for storing a cache line instruction, and a third field for storing information which is to be compared with information stored in the register(16:5 – 10, see flags and indicate state

of each cache location, i.e. cache line).

Regarding claim 19, the method of Claim 18 wherein the third field is programmed with memory addresses (FIG. 6, see 100 and 106 and all associated text).

Regarding claim 20, the method of Claim 18 wherein the third field is programmed with memory instructions (FIG. 6, see 90 and all associated text).

Allowable Subject Matter

6. Claim 15 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

"... wherein-the cache control logic has priority flags for discriminating priority between an address cache hit and an instruction cache hit..."

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuck Kendall whose telephone number is 571-272-3698. The examiner can normally be reached on 10:00 am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ck.

Chuck Kendall 6/17/07